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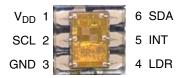
# Features

- Proximity Detection with an Integrated LED Driver in a Single Device
- Proximity Detection
  - Programmable Number of IR Pulses
  - Programmable Current Sink for the IR LED — No Limiting Resistor Needed
  - Programmable Interrupt Function with Upper and Lower Threshold
  - Covers a 2000:1 Dynamic Range
- Programmable Wait Timer
  - Programmable from 2.72 ms to > 8 Seconds
  - Wait State 65 μA Typical Current
- I<sup>2</sup>C Interface Compatible
  - Up to 400 kHz (I<sup>2</sup>C Fast Mode)
  - Dedicated Interrupt Pin
- Small 2 mm × 2 mm ODFN Package
- Sleep Mode 2.5 µA Typical Current

# TSL2671 DIGITAL PROXIMITY DETECTOR

TAOS118 - JANUARY 2011





Package Image Not Actual Size

# Applications

- Cell Phone Touch Screen Disable
- Notebook/Monitor Security
- Automatic Speakerphone Enable
- Automatic Menu Popup

# Description

The TSL2671 family of devices provides a complete proximity detection system and digital interface logic in a single 6-pin package. The device includes a digital proximity sensor with integrated LED driver for the required external IR LED. The proximity function offers a wide range of performance, with four programmable LED drive currents and a pulse repetition range of 1 to 32 pulses. The proximity detection circuitry compensates for ambient light, allowing it to operate in environments ranging from bright sunlight to dark rooms. This wide dynamic range also allows operation in short-distance detection applications behind dark glass, such as cell phones. An internal state machine provides the ability to put the device into a low-power mode for very low average power consumption.

The proximity function specifically targets near-field proximity applications. In cell phones, for example, the proximity detection function can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at the high repetition rate needed when answering a phone call. This provides both improved *green* power saving capability and the added security to lock the screen when the user may accidently deploy a touch.

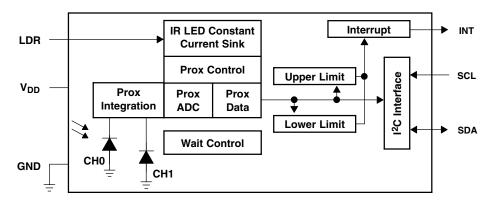
Communication with the device is accomplished through a simple two-wire I<sup>2</sup>C interface with data rates up to 400 kHz. An interrupt output pin is provided for connection to the host processor. This interrupt pin can be used to eliminate the need to poll the device on a repetitive basis. There is also a digital filter that compares the proximity ADC results to programmed values so that an interrupt is generated only upon a proximity event.

The TSL2671 is supplied in a very small form factor 2-mm  $\times$  2-mm, 6-pin optical package, requiring very little PCB area. Also, the package height is only 0.65 mm high, which makes the TSL2671 suitable for very thin mechanical applications.

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## **Functional Block Diagram**



## **Detailed Description**

The TSL2671 light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I<sup>2</sup>C interface. Each device combines a Channel 0 photodiode (CH0), which is responsive to both visible and infrared light, and a channel 1 photodiode (CH1), which is responsive primarily to infrared light. Proximity detection can occur using either or both photodiodes. Two integrating ADCs simultaneously convert the amplified photodiode currents into a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers.

Proximity detection requires only a single external IR LED. An internal LED driver can be configured to provide a constant current sink of 12.5 mA, 25 mA, 50 mA, or 100 mA of current. No external current limiting resistor is required. The number of proximity LED pulses can be programmed from 1 to 255 pulses. Each pulse has a 16-µs period. This LED current, coupled with the programmable number of pulses, provides a 2000:1 contiguous dynamic range.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I<sup>2</sup>C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a proximity value. An interrupt is generated when the value of a proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt.

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TERM	TERMINAL			
NAME	NO.	TYPE	TYPE DESCRIPTION	
GND	3		Power supply ground. All voltages are referenced to GND.	
INT	5	0	Interrupt — open drain.	
LDR	4	0	LED driver for proximity emitter — up to 100 mA, open drain.	
SCL	2	I	I <sup>2</sup> C serial clock input terminal — clock signal for I <sup>2</sup> C serial data.	
SDA	6	I/O	I <sup>2</sup> C serial data I/O terminal — serial data I/O for I <sup>2</sup> C.	٠. (
V <sub>DD</sub>	1		Supply voltage.	

#### Terminal Functions

#### **Available Options**

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TSL26711	0x39	FN–6	I <sup>2</sup> C Vbus = V <sub>DD</sub> Interface	TSL26711FN
TSL26713	0x39	FN–6	I <sup>2</sup> C Vbus = 1.8 V Interface	TSL26713FN
TSL26715	0x29	FN–6	I <sup>2</sup> C Vbus = V <sub>DD</sub> Interface	TSL26715FN
TSL26717	0x29	FN–6	I <sup>2</sup> C Vbus = 1.8 V Interface	TSL26717FN

## Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>DD</sub> (see Note 1)	
Digital output voltage range, Vo	
Digital output current, IO	
Storage temperature range, T <sub>stg</sub>	
ESD tolerance, human body model	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

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# **Recommended Operating Conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub>	2.6	3	3.6	V
Supply voltage accuracy, V <sub>DD</sub> total error including transients	-3		3	%
Operating free-air temperature, T <sub>A</sub>	-30		70	°C



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# Operating Characteristics, $V_{DD}$ = 3 V, $T_A$ = 25°C (unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT			
		Active — LDR pulse off		175	250			
I <sub>DD</sub>	Supply current	Wait mode		65		μA		
		Sleep mode		2.5	4			
		3 mA sink current	0		0.4			
V <sub>OL</sub>	DL INT, SDA output low voltage	IN I, SDA output low voltage	6 mA sink current	6 mA sink current	0		0.6	V
I <sub>LEAK</sub>	Leakage current, SDA, SCL, INT pins		-5		5	μΑ		
I <sub>LEAK</sub>	Leakage current, LDR pin			± 10		μA		
		TSL26711, TSL26715	0.7 V <sub>DD</sub>					
V <sub>IH</sub>	SCL, SDA input high voltage	TSL26713, TSL26717	1.25			V		
v		TSL26711, TSL26715			0.3 V <sub>DD</sub>	v		
VIL	SCL, SDA input low voltage	TSL26713, TSL26717			0.54	V		

# Proximity Characteristics, $V_{DD} = 3 V$ , $T_A = 25^{\circ}C$ , PEN = 1 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	CONDITION	MIN	ТҮР	MAX	UNIT
$I_{DD}$	Supply current	LDR pulse on			3		mA
	ADC conversion time step size	PTIME = 0xFF		2.58	2.72	2.9	ms
	ADC number of integration steps			1		256	steps
	ADC counts per step	PTIME = 0xFF		0		1023	counts
	IR LED pulse count			0		255	pulses
	Pulse period	6			16.3		μs
	Pulse — LED on time				7.2		μs
			PDRIVE=0	75	100	125	
		I <sub>SINK</sub> sink current @ 600 mV,	PDRIVE=1		50		
	LED Drive	LDR pin	PDRIVE=2		25		mA
			PDRIVE=3		12.5		
	Operating distance (See note 1)				18		inches

NOTE 1: Proximity Operating Distance is dependent upon emitter properties and the reflective properties of the proximity surface. The nominal value shown uses an IR emitter with a peak wavelength of 850 nm and a 20° half angle. The proximity surface used is 90% reflective (white surface) 16 × 20-inch Kodak Gray Card. 60 mw/SR, 100 mA, 64 pulses, open view (no glass). Note: Greater distances are achievable with appropriate system considerations.

# Wait Characteristics, $V_{DD} = 3 V$ , $T_A = 25^{\circ}C$ , WEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
Wait step size	WTIME = 0xFF		2.58	2.72	2.9	ms
Wait number of integration steps			1		256	steps



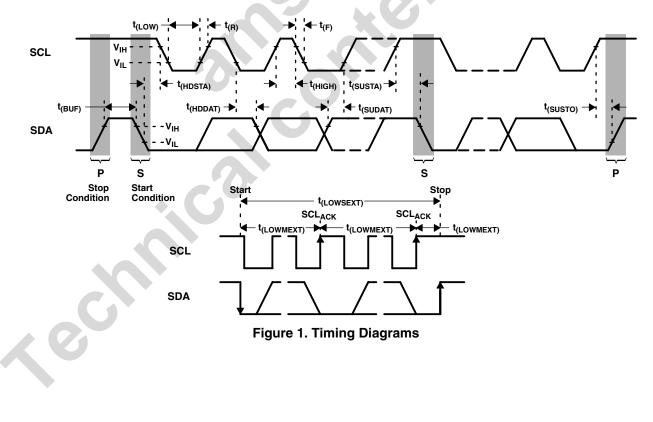
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	PARAMETER <sup>†</sup>	TEST CONDITIONS	MIN	TYP MA	xι	JNIT
f <sub>(SCL)</sub>	Clock frequency (I <sup>2</sup> C only)		0	40	00 I	kHz
t <sub>(BUF)</sub>	Bus free time between start and stop condition		1.3			μs
t <sub>(HDSTA)</sub>	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			μs
t <sub>(SUSTA)</sub>	Repeated start condition setup time		0.6			μs
t(SUSTO)	Stop condition setup time		0.6			μs
t <sub>(HDDAT)</sub>	Data hold time		0			μs
t <sub>(SUDAT)</sub>	Data setup time		100			ns
t <sub>(LOW)</sub>	SCL clock low period		1.3			μs
t <sub>(HIGH)</sub>	SCL clock high period		0.6			μs
t <sub>F</sub>	Clock/data fall time			30	0	ns
t <sub>R</sub>	Clock/data rise time			30	0	ns
Ci	Input pin capacitance				0	pF

# AC Electrical Characteristics, $V_{DD} = 3 V$ , $T_A = 25^{\circ}C$ (unless otherwise noted)

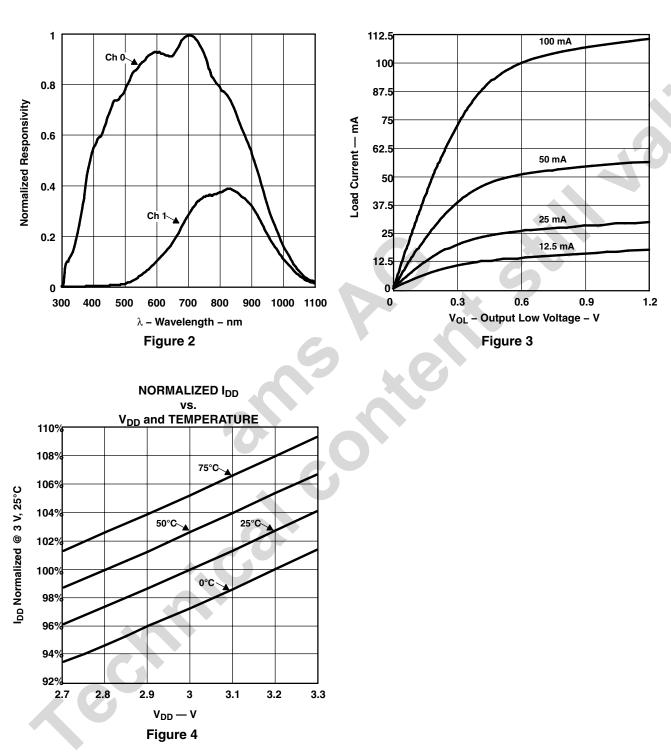
<sup>†</sup> Specified by design and characterization; not production tested.



# PARAMETER MEASUREMENT INFORMATION

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# **TYPICAL CHARACTERISTICS**



SPECTRAL RESPONSIVITY

LDR OUTPUT COMPLIANCE



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# **PRINCIPLES OF OPERATION**

#### **System State Machine**

The device provides control of proximity detection and power management functionality through an internal state machine. After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then cycle through the Proximity and Wait states. If these states are enabled, the device will execute each function. If the PON bit is set to a 0, the state machine will continue until the current conversion is complete and then go into a low-power sleep mode.

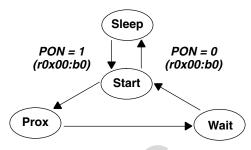


Figure 5. Simplified State Diagram

**NOTE:** In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0x00, bit 0. This is represented as *PON (r0x00:b0)*.

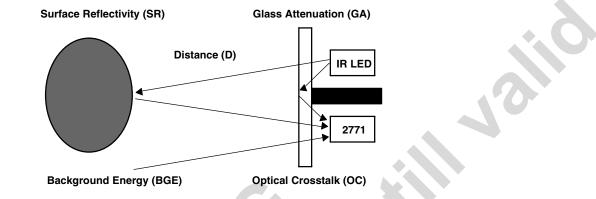




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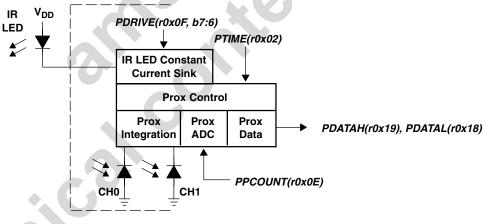
#### **Proximity Detection**

Proximity sensing uses an external light source (generally an infrared emitter) to emit light, which is then viewed by the integrated light detector to measure the amount of reflected light when an object is in the light path (Figure 6). The amount of light detected from a reflected surface can then be used to determine an object's proximity to the sensor.



**Figure 6. Proximity Detection** 

The device has controls for the number of IR pulses (PPCOUNT), the integration time (PTIME), the LED drive current (PDRIVE), and the photodiode configuration (PDIODE) (Figure 7). The photodiode configuration can be set to CH1 diode (recommended), CH0 diode, or a combination of both diodes. At the end of the integration cycle, the results are latched into the proximity data (PDATAx) registers.





The LED drive current is controlled by a regulated current sink on the LDR pin. This feature eliminates the need to use a current limiting resistor to control LED current. The LED drive current can be configured for 12.5 mA, 25 mA, 50 mA, or 100 mA. For higher LED drive requirements, an external P type transistor can be used to control the LED current.



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The number of LED pulses can be programmed to any value between 1 and 255 pulses as needed. Increasing the number of LED pulses at a given current will increase the sensor sensitivity. Sensitivity grows by the square root of the number of pulses. Each pulse has a  $16-\mu$ s period.

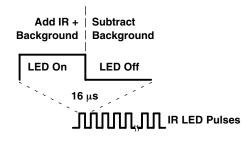
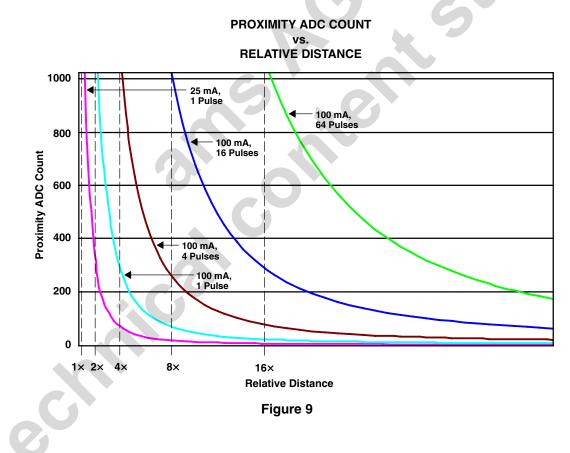


Figure 8. Proximity IR LED Waveform

The proximity integration time (PTIME) is the period of time that the internal ADC converts the analog signal to a digital count. It is recommend that this be set to a minimum of PTIME = 0xFF or 2.72 ms.

The combination of LED power and number of pulses can be used to control the distance at which the sensor can detect proximity. Figure 9 shows an example of the distances covered with settings such that each curve covers  $2\times$  the distance. Counts up to 64 pulses provide a  $16\times$  range.





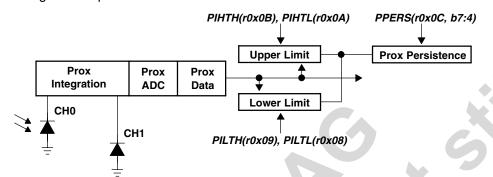
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#### Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for a proximity value. The interrupt mode is determined by the state of the PIEN field in the ENABLE register.

Two 16-bit-wide interrupt threshold registers allow the user to define upper and lower threshold limits. An interrupt can be generated when the proximity data (PDATA) exceeds the upper threshold value (PIHTx) or falls below the lower threshold (PILTx).

To further control when an interrupt occurs, the device provides an interrupt persistence feature. This feature allows the user to specify a number of conversion cycles for which an event exceeding the proximity interrupt threshold must persist (PPERS) before actually generating an interrupt. See the register descriptions for details on the length of the persistence.





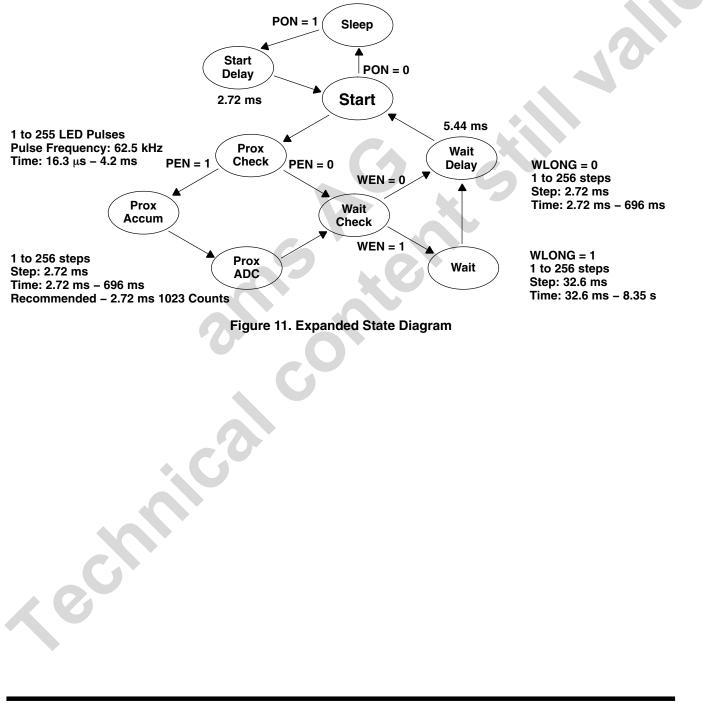
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#### **State Diagram**

The following state diagram shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.72-ms Start Delay will occur before entering the start state. If the PEN bit is set, the state machine will step through the proximity accumulate, then proximity ADC conversion states. As soon as the conversion is complete, the state machine will move to the Wait Check state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will move to the 2.72-ms Wait Delay state before returning to the Start state.

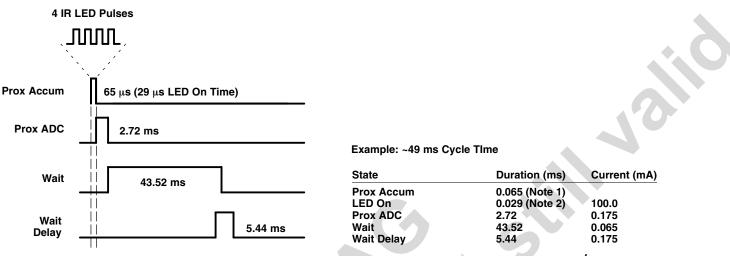




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## **Power Management**

Power consumption can be controlled through the use of the wait state timing because the wait state consumes only 65  $\mu$ A of power. Figure 14 shows an example of using the power management feature to achieve an average power consumption of 138  $\mu$ A current with four 100-mA pulses of proximity detection.



Average Current = (( $0.029 \times 100$ ) + ( $2.72 \times 0.175$ ) + ( $43.52 \times 0.065$ ) + ( $5.44 \times 0.175$ )) / 52 = 138  $\mu$ A

Note 1: Prox Accum = 16.3  $\mu$ s per pulse × 4 pulses = 65  $\mu$ s = 0.065 ms Note 2: LED On = 7.2  $\mu$ s per pulse × 4 pulses = 29  $\mu$ s = 0.029 ms

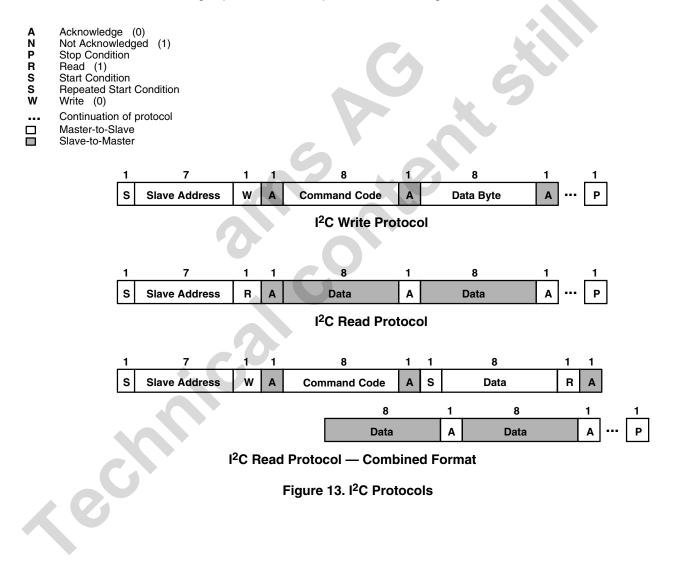
Figure 12. Power Consumption Calculations

#### I<sup>2</sup>C Protocol

Interface and control are accomplished through an I<sup>2</sup>C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I<sup>2</sup>C addressing protocol. Devices TSL26711 and TSL26713 are at slave address 0x39, while the TSL26715 and TSL26717 devices are at slave address 0x29.

The I<sup>2</sup>C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 13). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I<sup>2</sup>C bus protocol was developed by Philips (now NXP). For a complete description of the I<sup>2</sup>C protocol, please review the NXP I<sup>2</sup>C design specification at http://www.i2c-bus.org/references/.



TAOS118 – JANUARY 2011

#### **Register Set**

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	RESET VALUE
	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filter	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPCOUNT	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x18	PDATAL	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00

#### **Table 1. Register Address**

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I<sup>2</sup>C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.



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## **Command Register**

The command registers specifies the address of the target register for future write and read operations.

	7	6	5	4	3	2	1	0		
COMMAND	COMMAND	ТҮРЕ				ADD			]	$\mathbf{\lambda}$
FIELD	BITS				DES	CRIPTION				
COMMAND	7	Select Comma	nd Reg	ister. Must v	write as 1 when	addressing C	OMMAND reg	gister.		
TYPE	6:5	Selects type of	transa	ction to follow	w in subsequen	t data transfe	rs:			
		FIELD VALUE	<u>.</u>			DESCRIP	TION			
		00			Repea	ated byte prot	ocol transactio	on		
		01		Auto-increment protocol transaction						
		10			F	Reserved — [	)o not use			
		11			Special fu	unction — See	e description b	below		
		Transaction typ Transaction typ	be 00 w be 01 w	ill repeatedly ill provide ar	/ read the same auto-incremen	e register with It function to r	each data acc ead successiv	cess. ve register b	ytes.	
ADD 4:0 Address register/special function register. Depending on the transaction type, see above, this field e specifies a special function command or selects the specific control-status-register for following write read transactions:						, this field eithe owing write ar	er nd			
		FIELD VALUE				DESCRIP	TION			
		00000				Normal — n	o action			
		00101				Proximity inte	rupt clear			
		Proximity Intern	rupt Cle	ar clears an	y pending proxi	mity interrupt.	This special	function is	self clearing.	

#### Table 2. Command Register

# Enable Register (0x00)

The ENABLE register is used to power the device on/off, enable functions, and interrupts.

#### Table 3. Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	Rese	erved	PIEN	Reserved	WEN	PI	EN	PON	Address 0x00
FIELD	BITS				DESC	RIPTION			
Reserved	7:6	Reserved.	Write as 0.						
PIEN	5	Proximity in	terrupt mask.	When assert	ed, permits pr	oximity interr	upts to be ge	enerated.	
Reserved	4	Reserved.	Write as 0.						
WEN	3	Wait Enable wait timer.	e. This bit ac	tivates the wai	t feature. Wri	ting a 1 activa	ates the wait	timer. Writing	a 0 disables the
PEN	2:1	Proximity en disables pro	nable. These oximity. The <sup>v</sup>	e bits activate t Wait Time regi	he proximity f ster should be	unction. Writ configured b	ing a 11b ena efore asserti	ables proximity ng proximity e	y. Writing a 00b enable.
PON <sup>1, 2</sup>	0	Power ON. a 1 activate	This bit actives the oscillator	vates the interr or. Writing a 0	al oscillator to disables the o	o permit the ti oscillator.	mers and AD	C channel to	operate. Writing

NOTES: 1. See Power Management section for more information.

2. A minimum interval of 2.72 ms must pass after PON is asserted before proximity can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

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### Proximity Time Control Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.72 ms increments. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

### Table 4. Proximity Time Control Register

FIELD	BITS		DESCRIPTION								
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT						
		0xFF	1	2.72 ms	1023						

#### Wait Time Register (0x03)

Wait time is set 2.72 ms increments unless the WLONG bit is asserted, in which case the wait times are  $12 \times$  longer. WTIME is programmed as a 2's complement number.

FIELD	BITS	DESCRIPTION						
WTIME	7:0	REGISTER VALUE	WAIT TIME	TIME (WLONG = 0)	TIME (WLONG = 1)			
		0xFF	1	2.72 ms	0.032 sec			
		0xB6	74	201 ms	2.4 sec			
		0x00	256	696 ms	8.3 sec			

NOTE: The Wait Time register should be configured before PEN is asserted.

# Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0A	7:0	Proximity high threshold lower byte
PIHTH	0x0B	7:0	Proximity high threshold upper byte

#### **Table 6. Proximity Interrupt Threshold Registers**



#### Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time.

	7	6	5 4	3	2	1	0				
PERS	PPERS				Reserved						
FIELD	BITS		DESCRIPTION								
PPERS	7:4	Proximity interr	upt persistence.	Controls rate of p	oximity interr	upt to the hos	t processor.				
		FIELD VALU	E MEANING	11	NTERRUPT P	PERSISTENC	E FUNCTION				
		0000		Every proximity	cycle genera	tes an interrup	ot				
		0001	1	1 proximity valu	e out of range	e					
		0010	2	2 consecutive p	roximity value	es out of range					
		1111	15	15 consecutive	proximity valu	ues out of rang	je				
Reserved	3:0	Default setting	is 0x00.								

#### Table 7. Persistence Register

## Configuration Register (0x0D)

The configuration register sets the wait long time.

# **Table 8. Configuration Register**

	7	6 5 4 3 2	1	0			
CONFIG		Reserved	WLONG	Reserved	Address 0x0D		
FIELD	BITS	DESCRIPTION					
Reserved	7:2	Reserved. Write as 0.					
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.					
Reserved	0	Reserved. Write as 0.					

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#### TAOS118 - JANUARY 2011

#### Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that will be transmitted. PPULSE defines the number of pulses to be transmitted at a 62.5-kHz rate.

While the value can be programmed up to 255 pulses, the practical limit of the device is 32 pulses. It is recommended that 32 or fewer pulses be used to achieve maximum signal-to-noise ratio.

# Table 9. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0		
PPULSE		PPULSE								
FIELD	BITS		DESCRIPTION							
PPULSE	7:0	Proximity Pu	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.							

# Control Register (0x0F)

The Control register provides four bits of control to the analog block. These bits control the diode drive current and diode selection functions.

	7	6 5	4	3	2 1	0	
CONTROL	PDRIV	E	PDIODE Reserved				Address 0x0F
FIELD	BITS			DES	CRIPTION		
PDRIVE	7:6	LED Drive Streng	th.				
		FIELD VALUE			LED STRENGTH		
		00	100 mA				
		01	50 mA				
		10	25 mA				
		11	12.5 mA				
PDIODE	5:4	Proximity Diode S	elect.				
		FIELD VALUE			DIODE SELECTION		
		00	Reserved				
		01	Proximity uses t	he Channel (	) diode		
		10	Proximity uses t	he Channel 1	1 diode		
		11	Proximity uses b	ooth diodes			
Reserved	3:0	Reserved. Write	oits as 0.				

#### Table 10. Control Register



TAOS118 - JANUARY 2011

## ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

				Table 11. I	D Register					
	7	6	5	4	3	2	1	0		
ID			Address 0x12	X						
FIELD	BITS	DESCRIPTION								
ID	7.0	Dort number	identification		0x00 =	0x00 = TSL26711 and TSL26715				
U	7:0	Part number	Part number identification 0x09 = TSL26713 and TSL26713							

#### Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

			Та	ble 12. Sta	tus Registe	er			
	7	6	5	4	3	2	1	0	
STATUS	Res	served	PINT			Reserved			Address 0x13
FIELD	BIT				DESCR				
Reserved	7:6	Reserved.							
PINT	5	Proximity In	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.						
Reserved	4:0	Reserved.							

# Proximity Data Registers (0x18 - 0x19h)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte I<sup>2</sup>C read transaction should be utilized with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

#### Table 13. Proximity Data Registers



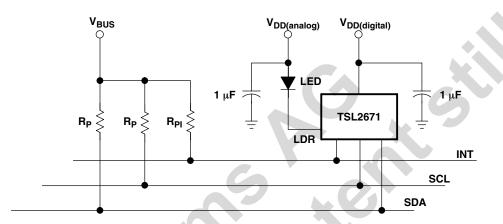
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# **APPLICATION INFORMATION: HARDWARE**

## **LED Driver Pin with Proximity Detection**

The application hardware circuit with proximity detection requires an LED connected as shown in Figure 14.  $V_{bat}$  may be an independent power source. The 1- $\mu$ F decoupling capacitors should be of the low-ESR type and be placed as close as possible to the load and  $V_{DD}$  to reduce noise. To maximize system performance, the use of PCB power and ground planes are recommended. If mounted on a flexible circuit, the power and ground traces back to the PCB should be sufficiently wide enough to have a low resistance, such as < 1 $\Omega$ .

The I<sup>2</sup>C bus protocol was developed by Philips (now NXP). The pull-up resistor value (R<sub>P</sub>) is a function of the I<sup>2</sup>C bus speed, the supply voltage, and the capacitive bus loading. Users should consult the NXP I<sup>2</sup>C design specification (http://www.i2c-bus.org/references/) for assistance. With a lightly loaded bus running at 400 kbps and V<sub>DD</sub> = 3 V, 1.5-k $\Omega$  resistors have been found to be viable.



#### Figure 14. Application Hardware Circuit for Proximity Sensing with Internal LED Driver

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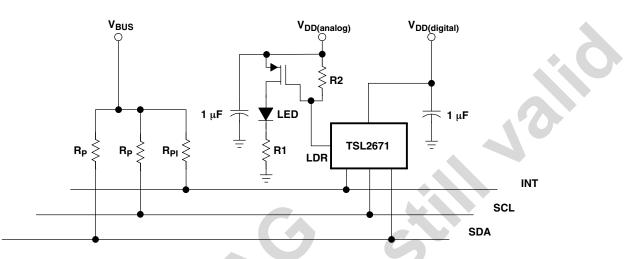
The power supply connection — PCB routing and supply decoupling — has a significant effect on proximity performance. Contact TAOS or see the application notes available at www.TAOSinc.com for power supply guidance.

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# **APPLICATION INFORMATION: HARDWARE**

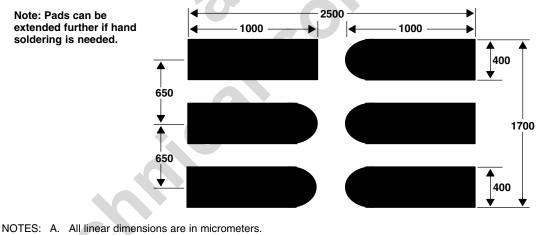
If the hardware application requires more than 100 mA of current to drive the LED, then an external transistor should be used. Note, R2 should be sized adequately to bias the gate voltage given the LDR current mode setting. See Figure 15.





## PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in Figure 16.



B. This drawing is subject to change without notice.

Figure 16. Suggested FN Package PCB Layout



TAOS118 - JANUARY 2011

**MECHANICAL DATA PACKAGE FN Dual Flat No-Lead TOP VIEW** Pin 1 Marker **PIN OUT** TOP VIEW PIN 1 6 SDA V<sub>DD</sub> 1 SCL 2 5 INT 2000 ± 75 GND 3 4 LDR 2000 **Photo-Active Area** ± 75 **END VIEW** SIDE VIEW 650 ± 50 203 ± 8 Seating Plane 650 ←→ 300 **BOTTOM VIEW** ± 50 650 300 ± 50 PIN 1 750 ± 150 Lead Free

NOTES: A. All linear dimensions are in micrometers. Dimension tolerance is  $\pm\,20\,\mu\text{m}$  unless otherwise noted.

- B. The photodiode active area is 466  $\mu$ m square and its center is 140  $\mu$ m above and 20  $\mu$ m to the right of the package center. The die placement tolerance is  $\pm$  75  $\mu$ m in any direction.
- C. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
- D. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
- E. This package contains no lead (Pb).
- F. This drawing is subject to change without notice.

#### Figure 17. Package FN — Dual Flat No-Lead Packaging Configuration

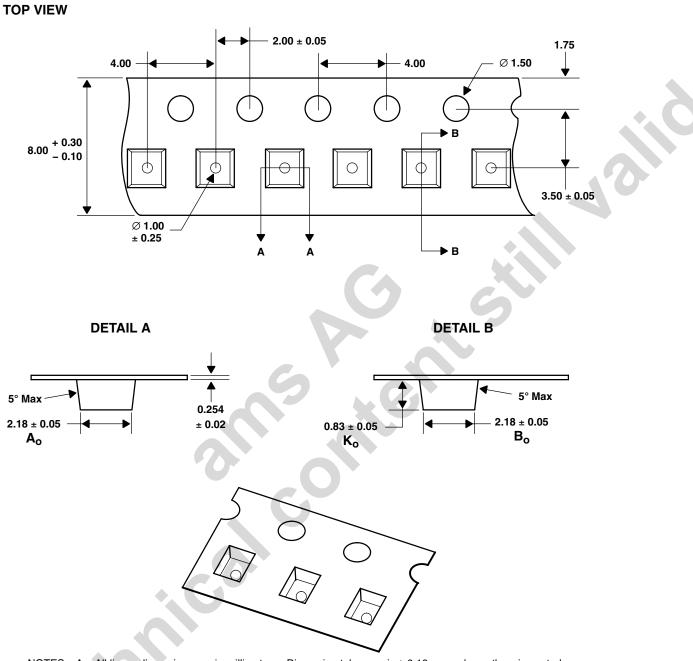
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- NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is  $\pm$  0.10 mm unless otherwise noted.
  - B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
  - C. Symbols on drawing A<sub>o</sub>, B<sub>o</sub>, and K<sub>o</sub> are defined in ANSI EIA Standard 481–B 2001.
  - D. Each reel is 178 millimeters in diameter and contains 3500 parts.
  - E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481-B.
  - F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
  - G. This drawing is subject to change without notice.

Figure 18. Package FN Carrier Tape

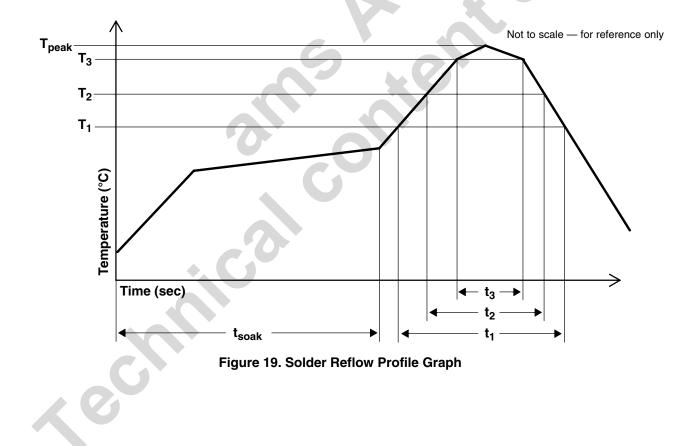
TAOS118 - JANUARY 2011

# MANUFACTURING INFORMATION

The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these test are detailed below.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t <sub>soak</sub>	2 to 3 minutes
Time above 217°C (T1)	t <sub>1</sub>	Max 60 sec
Time above 230°C (T2)	t <sub>2</sub>	Max 50 sec
Time above T <sub>peak</sub> -10°C (T3)	t <sub>3</sub>	Max 10 sec
Peak temperature in reflow	T <sub>peak</sub>	260°C
Temperature gradient in cooling		Max –5°C/sec





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# MANUFACTURING INFORMATION

#### **Moisture Sensitivity**

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The Moisture Barrier Bags should be stored under the following conditions:

Temperature Range	< 40°C
Relative Humidity	< 90%
Total Time	No longer than 12 months from the date code on the aluminized envelope if
	unopened.

Rebaking of the reel will be required if the devices have been stored unopened for more than 12 months and the Humidity Indicator Card shows the parts to be out of the allowable moisture region.

Opened reels should be used within 168 hours if exposed to the following conditions:

Temperature Range< 30°C</th>Relative Humidity< 60%</td>

If rebaking is required, it should be done at 50°C for 12 hours.

The FN package has been assigned a moisture sensitivity level of MSL 3.



TAOS118 - JANUARY 2011

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**Green (RoHS & no Sb/Br)** TAOS defines *Green* to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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